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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,512	02/17/2004	Tai-Chun Huang	TS03-461	1383
42717	7590	04/06/2005	EXAMINER	
HAYNES AND BOONE, LLP 901 MAIN STREET, SUITE 3100 DALLAS, TX 75202			CHU, CHRIS C	
			ART UNIT	PAPER NUMBER
			2815	

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/780,512

Applicant(s)

HUANG ET AL.

Examiner

Chris C. Chu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 21 January 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1 - 25 is/are pending in the application.
- 4a) Of the above claim(s) 4, 9 - 15 and 24 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1 - 3, 5 - 8, 16 - 23 and 25 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 February 2004 is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>4/29/04</u> . | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Election/Restrictions***

1. Applicant's election of Group I and Species IV (Fig. 8B) in the reply filed on January 21, 2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

2. Applicant elected claims: 1, 2, 4 – 8, 16 – 22, 24 and 25. However, a quick review of Fig. 8B shows that the claims 4 and 24 do not read on Species IV, but claims 3 and 23 are read on Species IV. Therefore, claims 4, 9 – 15 and 24 have been treated as a non-elected Species and are hereby withdrawn from consideration consistent with the election that filed on January 21, 2005 as addressed above.

In claims 4 and 24, the limitation “said first width of said seal ring covering the whole of said corner portion of said seal ring” does not read on Fig. 8B.

### ***Drawings***

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: the reference number “12” is not disclosed in the specification of instant invention.

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4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation in claim 8, “wherein devices involved in temperature testing may be located outside of said seal ring” must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Objections*

5. Claims 1 – 25 are objected to because of the following informalities:

(A) In claim 1:

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- In line 5, "lines wherein" should be --lines, wherein--.
  - In line 5, "lines and wherein" should be --lines, wherein--.
- (B) Claims 1 – 25, need a comma after claim number (i.e., Claim 1, wherein).
- (C) In claim 19:
- line 4, "lines wherein" should be --lines, wherein--.
  - line 4, "lines wherein said plurality" should be -- lines and wherein said plurality--

Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 2, 6, 8, 20 and 23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- (A) In claims 2 and 20, the term "sharp" is a relative term which renders the claim indefinite. The term "sharp" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.
- (B) In claim 6, the term "about" is a relative term which renders the claim indefinite. The term "about" is not defined by the claim, the specification does not provide a

standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

- (C) In claim 8, the phrase "may be" renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention.

See MPEP § 2173.05(d).

- (D) In claim 23, it is unclear what the applicant regards as "said first width of said seal ring covering a portion of said corner portion of said seal ring". That is, how could the seal ring cover a portion of itself? Thus, the claim cannot be understood.

### *Claim Rejections - 35 USC § 102*

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

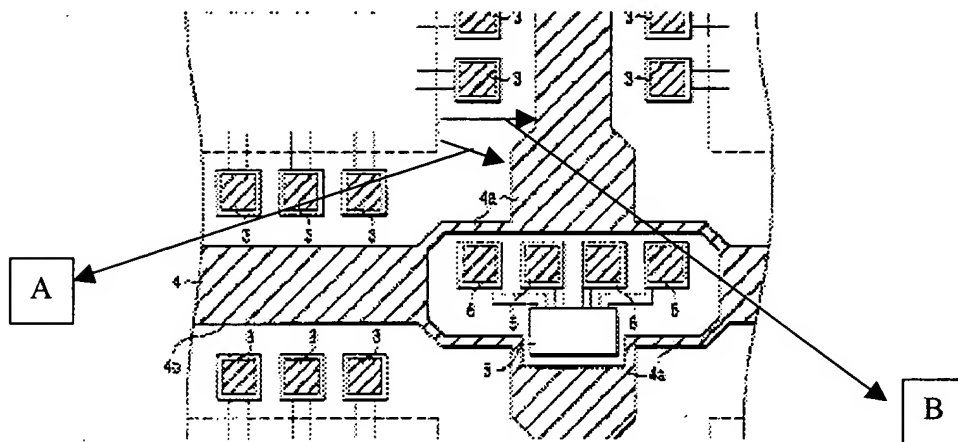
9. Claims 16, 18, 21 – 23 and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsuji et al. (U. S. Pat. No. 6,291,835).

Regarding claim 16, Tsuji et al. discloses in Figure and column 2, lines 45 – 67 a semiconductor device (1; column 2, line 46) comprising:

- semiconductor device structures (any structures inside of the element 4) formed in and on a substrate; and
- a seal ring (4; column 1, line 58 – 60 and Figure show corners and sides of four chips that are separated by the lines 4. Thus, the lines 4 that cover the every corners and

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- sides of a single chip's board lines read as a continuous seal ring.) enclosing said semiconductor device structures forming a single die (2; column 2, line 51),
- wherein a first distance (A) between said semiconductor device structures and a corner portion of said seal ring is smaller than a second distance (B) between said semiconductor device structures and an edge portion of said seal ring (see Figure below).



Regarding claim 18, Tsuji et al. discloses in Figure said semiconductor device structures including all active devices of said semiconductor device (column 2, lines 44 – 51) except for devices used for temperature testing (Since applicant does not specifically claim that the “devices used for temperature testing” is for a semiconductor die, a reasonable interpretation of the term “devices used for temperature testing” includes any thermo-devices, e.g., thermometers or heat sensors for reactors or furnace or air conditioner, etc., that locate outside of the die and inside of a factory).

Regarding claim 21, Tsuji et al. discloses in Figure said corner portion (4a; column 2, line 54) of said seal ring (4) having a first width and wherein said edge portion (4b; column 2, line

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55) of said seal ring has a second width wherein said first width is wider than said second width (see Figure and column 2, lines 54 – 56).

Regarding claim 22, Tsuji et al. discloses in Figure said first width being “about” 1.5 times said second width or greater (column 2, lines 61 – 63).

Regarding claim 23, Tsuji et al. discloses in Figure said first width of said seal ring covering a portion of said corner portion of said seal ring (see the Figure).

Regarding claim 25, Tsuji et al. discloses in Figure one or more slots or holes (at the area where the elements 5 and 6 are formed) being formed in said corner portion (4a) of said seal ring (4).

### ***Claim Rejections - 35 USC § 103***

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

11. Claims 1 – 3, 5 – 8, 17, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuji et al. (U. S. Pat. No. 6,291,835) in view of Ma et al. (U. S. Pat. No. 6,509,622).

Regarding claim 1, Tsuji et al. discloses in Figure and column 2, lines 45 – 67 a seal ring structure comprising:

- a substrate (1; column 2, line 46);



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- a plurality of metal lines (4a and 4b; column 2, lines 52 – 63) formed overlying said substrate; and
  - o wherein said plurality of metal lines (4a and 4b) forms a continuous seal ring (column 1, line 58 – 60 and Figure show corners and sides of four chips that are separated by the lines 4. Thus, the lines 4 that cover the every corners and sides of a single chip's board lines read as a continuous seal ring.) around a die (2; column 2, line 51) and
  - o wherein a first width (4a; column 2, line 54) of said metal lines at a corner of said die is wider (column 2, lines 52 – 63) than a second width (4b; column 2, lines 55 – 56) of said metal lines at edges of said die (see the Figure).

While Tsuji et al. teaches a plurality of metal lines on top layer of the substrate, Tsuji et al. does not appear to provide a plurality of layers of metal lines and a plurality of metal vias. Ma et al. teaches in e.g., Fig. 2 a plurality of layers of metal lines (205 – 209; column 3, lines 29 – 30) formed overlying a substrate and a plurality of metal vias (211 – 215; column 3, lines 30 – 32) through intermetal dielectric layers (column 3, lines 40 – 45) between the layers of metal lines, wherein said metal vias (211 – 215) interconnect said metal lines (see e.g., Fig. 2) and wherein said plurality of layers of interconnected metal lines forms a continuous seal ring (105 in Fig. 1A and column 2, lines 55 – 56) around a die (103; column 2, line 55). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the plurality of layers of metal lines and the plurality of metal vias between the metal lines and the substrate of Tsuji et al. to decrease a mechanical failure of the devices or the interconnects due to

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a mechanical stress, such as interconnect shearing, by providing the high shear strengthened plurality of guard rings (column 1, lines 24 – 34 and column 4, lines 1 – 2).

Regarding claim 2, Tsuji et al. discloses in Figure said metal lines (4a and 4b) being parallel to said edges (the broken lines in the element 1) of said die (2) and wherein said metal lines are sloped at said corner of said die so that said metal lines do not have a “sharp” corner (see Figure).

Regarding claim 3, Tsuji et al. discloses in Figure said first width (4a) of said metal lines covering a portion of said corner (see Figure).

Regarding claim 5, Tsuji et al. discloses in Figure one or more slots or holes (at the area where the elements 5 and 6 are formed) being formed in said first width (4a) of said metal lines at said corner (see Figure).

Regarding claim 6, Tsuji et al. discloses in Figure said first width (4a) being “about” 1.5 times said second width (4b) or greater (column 2, lines 61 – 63).

Regarding claim 7, Tsuji et al. discloses in Figure semiconductor device structures within said die (2) wherein a first distance between said semiconductor device structures and a corner portion of said seal ring is smaller than a second distance between said semiconductor device structures and an edge portion of said seal ring.

Regarding claim 8, Tsuji et al. discloses in Figure all active semiconductor device structures in said die are located within said seal ring and wherein devices involved in temperature testing (i.e., thermometers or heat sensors in the wafer assembly process in a semiconductor factory) may be located outside of said seal ring (Since applicant does not specifically claim that the “devices involved in temperature testing” is for a semiconductor die, a

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reasonable interpretation of the term “devices involved in temperature testing” includes any thermo-devices, e.g., thermometers or heat sensors for reactors or furnace or air conditioner, etc., that locate outside of the die and inside of a factory).

Regarding claim 17, Ma et al. teaches in e.g., Fig. 2 semiconductor device structures (devices; column 2, lines 56 – 59) including gate electrodes, source and drain regions (since the devices include transistors, Ma et al. discloses the claimed structures), and a plurality of layers of interconnected conductive lines (201; column 3, lines 29 – 32).

Regarding claim 19, a further difference between Tsuji et al. and instant invention is said seal ring (4) comprising:

- a plurality of layers of metal lines formed on said substrate; and
- a plurality of metal vias through intermetal dielectric layers between said layers of metal lines
  - o wherein said metal vias interconnect said metal lines and
  - o wherein said plurality of layers of interconnected metal lines forms a continuous seal ring around said die.

Ma et al. teaches in e.g., Fig. 2 a plurality of layers of metal lines (205 – 209; column 3, lines 29 – 30) formed on a substrate and a plurality of metal vias (211 – 215; column 3, lines 30 – 32) through intermetal dielectric layers (column 3, lines 40 – 45) between the layers of metal lines, wherein said metal vias (211 – 215) interconnect said metal lines (see e.g., Fig. 2) and wherein said plurality of layers of interconnected metal lines forms a continuous seal ring (105 in Fig. 1A and column 2, lines 55 – 56) around a die (103; column 2, line 55). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the

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plurality of layers of metal lines and the plurality of metal vias between the metal lines and the substrate of Tsuji et al. to decrease a mechanical failure of the devices or the interconnects due to a mechanical stress, such as interconnect shearing, by providing the high shear strengthened plurality of guard rings (column 1, lines 24 – 34 and column 4, lines 1 – 2).

Regarding claim 20, Tsuji et al., as modified, discloses said interconnected metal lines being parallel to said edges of said die and wherein said interconnected metal lines are sloped at said corner of said die so that said interconnected metal lines do not have a “sharp” corner.

### *Conclusion*

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lin et al., Lee, Towle et al., Shirato et al., Chang et al., Tsuji, Hagihara and Yoneyama disclose a guard ring in a semiconductor device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 517-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.


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Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chris C. Chu  
Examiner  
Art Unit 2815

c.c.  
Thursday, March 24, 2005

  
GEORGE ECKERT  
PRIMARY EXAMINER